## REMARKS

This amendment is submitted in response to the final office action dated October 18, 2006 and the Advisory Action of January 18, 2007. Reconsideration and allowance of claims is requested. In this office action, claims 1-20 are considered and rejected as either anticipated by or obvious in view of Wilson (US Patent No. 5,557,734). These rejections are respectively traversed. In making these rejections, the Examiner has not accounted for several of the limitations of the claims. Claims 2, 16-18 are cancelled and new claims 21-24 are presented.

Claim 1, which is now combined with claim 2 to present a new claim 1, recites a plurality of data buses connected with a plurality cache memory units and an RXN adapted for processing data connected with the plurality of buses. In rejecting the claim, the Examiner fails to account for the requirement that the RXN be adapted for processing data. He reads the claims simply on the data busses that passively move data from a cache memory to a node, which does not comprise processing data in any reasonable context of the word.

As to claim 3, which recites a multiplexer for alternately connecting the data input with each of the plurality of buses, the Examiner reads this limitation on the multiplexers shown in figure 7 of Wilson. However, the multiplexers are only shown as part of a two level multiplexer for implementing a truth table processor and do not provide the function of alternately connecting a data input with each of the plurality of data buses as recited in claim 3.

Claim 12 recites, among other things, that a plurality of cache memory units is provided, each having a plurality of cache ports. The Examiner reads this on figure 5 of Wilson, which shows a single memory unit (MEM8) having two cache ports. The Examiner alleges these two ports may each be connected to one or more of the plurality of data buses. This rejection must fail on two levels. First, the reference does not show a plurality of cache memory units, each having a plurality of cache ports. Further, it is not established that more than one data bus is connected to a different one of the plurality of cache ports from each of the memory units.

Claim 7 recites that a plurality of data address generators simultaneously communicate a plurality data values to the plurality of data buses. The Examiner, in his rejection, reads this limitation on the teachings in Wilson related to cache memory MEM5. However, the Examiner interpreted the claims such that they can be rejected in view of the teachings in Wilson related only to or only MEM8. It is clear that MEM5 does not have the attributes required by claim 1. Therefore, the examiner cannot attribute a characteristic of MEM5 to a different memory MEM8 in Wilson when each cache memory described in the specification and covered by the claims of the present application provides all the functions recited in claim 7.

Claim 8 recites that the cache memory unit loads a plurality of data values of a plurality of different data buses with the data values being loaded from the different buses through the same cache port. The Examiner reads these limitations on teachings in the background section of Wilson concerning storing data in different caches. However, as previously argued, the Examiner already interpreted the claims such that they can be rejected in view of the teachings in Wilson related to only MEM8. Therefore, once again, the Examiner is limited to cache memory characteristics which can only been attributed to MEM8 and cannot now rely on the attributes of the other cache memories in Wilson without some teaching or suggestion in Wilson which would cause a person of skill in the art to combine the functions of these different cache memories. Further, as to all the other cache memories in the Wilson reference, they are only connected to a single data bus, as conceded by the Examiner in his rejection. Therefore this rejection must fail.

The arguments which are made with respect to claims 7 and 8 apply equally to claims 13, 15 and 16 of the present application.

Finally, with respect to claim 20, the claim recites simultaneously transferring a first subset of data values to a plurality of data buses. However, there is no such teaching in the Wilson reference, where each of the memories is connected to only a single data bus, as clearly shown in Fig. 5 and implicitly conceded by the Examiner in his rejection of claim 1.

Applicant has further extensively amended claims 12 and 20 to emphasize the novel approach presented at pages 11 and 12 and shown in Figure 7 of the present application for transposing a matrix. As pointed out in the application, the advantage of this operation, which is available through the structure claimed herein, is that the transposed matrix is created using sequential reads from the main memory and birth mode cache rights and does not require any complicated data address generation data storage data recording or the like, as would be required by either or both of the references cited by the Examiner. Further, the claimed configuration raises the speed of the transpose operations and consumes significantly less power. Applicant has further amended claim 1 and has proposed additional claims 21-24 to emphasize the further novel features of providing a cache memory comprising a plurality of cache units that is capable of being configured with the control words taken from the data cache to execute sequence of operations. Not only are the control words selectively transferred at very high speed to the reconfigurable processing node, but an index word is defined for selectively accessing any cache line in any of the memory units. Further, an access control word is defined in this system to enable highly efficient sequential accesses of frequently used control words. All of these features are clearly presented in the claims submitted herewith.

In view of these clear distinctions, reconsideration and allowance of the claims, is respectfully requested.

Respectfully submitted,

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